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Guidelines for measuring the threshold voltage (V_T) of SiC MOSFETs

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1 Numbers in square brackets refer to the Bibliography.

The text of this International Standard is based on the following documents:

Draft	Report on voting
47/2885/FDIS	47/2908/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

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- reconfirmed,
- withdrawn, or
- revised.

INTRODUCTION

This document is intended for use in the SiC power semiconductor and related power electronic industries and provides guidelines for measuring the threshold voltage (V_T) of SiC power devices.

Threshold voltage (V_T) is a key parameter in the evaluation of changes in the characteristics of physical stimulus such as voltage and/or temperature stress. Without accurately measuring threshold voltage, it is not possible to monitor how device characteristics are changed by the stress applied to a device.

SiC/SiO_2 interface of Silicon Carbide (SiC) Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is more complex than the Si/SiO_2 interface, which requires careful handling of traps in the device with regard to the change monitoring of characteristics.

The test methods provided in this document can be used as a guideline for measuring threshold voltage of SiC power device, focused on N-channel vertical structure MOSFET technologies. These three test methods can be applied for datasheet, process control, technology development, final tests and other usage.

GUIDELINES FOR MEASURING THE THRESHOLD VOLTAGE (V_T) OF SIC MOSFETS

1 Scope

This document gives guidance on V_T measurement methods and conditioning prior to V_T testing in SiC power MOSFETs to reduce or eliminate the effect of the aforementioned hysteresis. The method is applicable for PBTI testing, NBTI and threshold voltage changes caused by switching events are excluded from the scope.

SiC MOSFETs have threshold voltage hysteresis caused by transient trap effects, which impacts the evaluation of the actual the V_T shift caused by stress tests such as bias temperature instabilities (BTI) [2].

The test methods can be applied to the following:

a) N-channel SiC MOSFET (vertical structure);

b) the above in wafer and package levels.

2 Normative references

There are no normative references in this document.